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LAHIVE & COCKFIELD, LLP.
28 STATE STREET
BOSTON, MA 02109

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,196	NGO ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *18-27* is/are allowed.

6)☒ Claim(s) *1-8,10,12-17,28-30 and 32* is/are rejected.

7)☒ Claim(s) *9,11 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2005* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-32 are pending in the instant application.

Drawings

2. The drawings were received on April 20, 2005. These drawings are accepted by the Examiner.

Response to Arguments

3. In view of the amendments to the claims filed April 20, 2005, the prior art rejections set forth in the first office action dated March 10, 2005 have been withdrawn.

4. New art rejections are set forth below.

Claim Objections

5. Claims 10, 25 and 29 are objected to because of the following informalities:

Regarding claim 10, in line 2, "said propagation delay" should be replaced by –said amount of propagation delay", in line 4, "said propagation delay" should be replaced by –said amount of propagation delay--, and, in line 6, "said counter" is lacking antecedent basis.

Regarding claim 25, in line 2, "delay elements comprise" should be replaced by –delay elements each comprise--.

Regarding claim 29, the claim is objected to because it fails to further limit the parent claim 28. That is, the parent claim 29 already is limited to contain a detection circuit and a delay circuit.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-3, 6-8, 10, 13, 14, 28-20, and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Glenn et al (U.S. Pub. 2003/0002608; hereafter "Glenn")

Regarding claim 1, Glenn discloses a system for synchronous communication between a first integrated circuit (fig. 1, ref. 101; para. 0002) and a second integrated circuit (fig. 1, ref. 102) comprising: a synchronous interconnect structure (fig. 4) for correcting a timing alignment of a data signal (fig. 1, "DATA) and a source clock signal (fig. 1, "CLK") between said first integrated circuit and said second integrated circuit each time said data signal and said source clock signal are transmitted across said synchronous interconnect structure, wherein said synchronous interconnect structure comprises, a control circuit (fig. 4, ref. 405) to control an amount of propagation delay inserted into a first transmission path and a second transmission path (fig. 1, ref. 110), wherein said data signal propagates on said first transmission path and said source clock signal propagates on said second transmission path (fig. 1); and a phase-locked loop circuit (fig. 4, refs. 404-408) to provide said control circuit with a time varying signal (fig. 4, refs. 416 and 417) that indicates when the amount of propagation delay inserted into said first and second transmission paths should be inserted (para. 0044 and 0045).

Glenn discloses a phase locked loop circuit (fig. 4, refs. *the interconnections of 404-408*) which synchronizes said timing alignment by asserting a time dependent signal (fig. 4, refs. 416 and 417) aligned to said source clock signal to synchronize operation of said delay circuit (fig. 4, refs. 407 and 408; para. 0052) by the operative interconnection of the elements of the circuit. That is, the phase locked loop is the particular sequence and connection of the elements of the deskewing circuit. It is a phase locked loop because the phase comparison by the PHASE ADJUSTMENT UNIT (fig. 4, ref. 405) is operatively connected to the PHASE SHIFTERS (fig. 4, refs. 407 and 408) which are operatively coupled to the DATA SAMPLER (fig. 4, ref. 404) providing a time dependent signal which is operatively coupled to the PHASE ADJUSTMENT UNIT *in a loop*.

Regarding claim 2, Glenn discloses the limitations of claim 1 as applied above. Further, Glenn discloses that said control circuit and said phase-locked loop circuit are part of a receiver circuit of said synchronous interconnect structure (fig. 1, ref. 102).

Regarding claim 3, Glenn discloses the limitations of claim 2 as applied above. Further, Glen discloses a transmitter circuit (fig. 1, ref. 101) comprising a first transmitter for CLK (fig. 1) and a second transmitter for DATA (fig. 1) wherein said first transmitter asserts said source clock signal and said second transmitter asserts said data signal; and a first transmission line and a second transmission line (fig. 1), wherein said first transmission line interconnects said first transmitter and a first receiver (fig. 4, ref. 407) receiving said source clock signal and said second transmission line interconnects said second transmitter and a second receiver (fig. 4, ref. 408) receiving said data signal, wherein said first and second receivers are part of said receiver circuit.

Regarding claim 6, Glenn discloses the limitations of claim 1 as applied above. Further, Glenn discloses an integration sense amplifier (fig. 4, ref. 404) to integrate and sense a value of said data signal (fig. 4, ref. 415) after said correction of said timing alignment by said control circuit (fig. 4, ref. 405).

Regarding claim 7, Glenn discloses the limitations of claim 7 as applied above. Further, Glenn discloses that the amount of propagation delay inserted into said first transmission path can have a value different from the amount of propagation delay inserted into said second transmission path because the delays are implemented separately by separate phase shifters (fig. 4, refs. 407 and 408; para. 0044).

Regarding claim 8, Glenn discloses the limitations of claim 1 as applied above. Further, Glenn discloses that said control circuit comprises a detection circuit (fig. 5, ref. 501) to determine and assert a correction signal (fig. 1, refs. 503 and 504) if the amount of propagation delay inserted into said first and said second transmission paths needs adjustment; and a delay circuit (fig. 4, refs. 407 and 408) that inserts the amount of propagation delay into said first and said second transmission paths based on said time varying signal (fig. 4, refs. 416 and 417) provided by said phase-locked loop circuit and said correction signal (fig. 4, refs. 410 and 411) asserted by said detection circuit.

Regarding claim 10, Glenn discloses the limitations of claim 8 as applied above. Further, Glenn discloses that the delay circuit comprises a first delay element (fig. 4, ref. 407) to insert said propagation delay into said first transmission path (fig. 4, ref. 412) within said receiver; a second delay element (fig. 4, ref. 408) to insert said propagation delay into said second transmission path (fig. 4, ref. 413) within said receiver; and a

finite state machine or filter (fig. 5, refs. 502a and 502b) to interpret and control the amount of propagation delay inserted into said first and second transmission paths by said delay circuit (para. 0050).

Regarding claim 13, Glenn discloses the limitations of claim 1 as applied above. Further, Glenn discloses that said first integrated circuit (fig. 1, ref. 101) and said second integrated circuit (fig. 1, ref. 102) each comprise a microprocessor or, as broadly as claimed, a semiconductor ("micro") which processes data ("processor") (para. 0002).

Regarding claim 14, Glenn discloses the limitations of claim 1 as applied above. Further, according to the disclosure of Glenn, the phase locked loop could alternatively be considered a delay locked loop because the loop (fig. 4, refs. 407, 408, 406, 404, and 405) utilizes phase shifters or phase delays (fig. 4, refs. 407 and 408) to implement the loop.

Regarding claim 28, Glenn discloses a deskewing circuit (fig. 4) to perform a timing alignment of a synchronous point-to-point signal (fig. 4, refs. 412 and 413) on a per signal basis comprising, a control circuit (fig. 4, ref. 405) to control said timing alignment of said synchronous point-to-point signal, wherein the control circuit comprises: a detection circuit (fig. 5, ref. 501) detecting a phase differential between a first data signal (fig. 4, ref. 413) of said synchronous point-to-point signal and a source clock-signal (fig. 4, refs. 401-403) of said synchronous point-to point signal; and a delay circuit (fig. 4, refs. 407 and 408) delaying both said first data signal and said source clock-signal based on an output signal (fig. 4, refs. 410 and 411) of said detection circuit. As broadly as claimed, the detection circuit detects a phase differential between

the first signal (fig. 4, DATA) and a source clock signal (fig. 4, "CLOCK) by sampling the first signal by the source clock signal which is comprised of three clock phases (fig. 4, refs. 401-403; "PRE CLK", "CLK", "POST CLK") to determine if the source clock signal ("CLK") has a leading or lagging phase differential with respect to the first signal (para. 0052).

Regarding claim 29, Glenn discloses the limitations of claim 28 as applied above. Glenn further discloses that said control circuit further comprises a detection circuit and a delay circuit as applied to claim 28 above.

Regarding claim 30, Glenn discloses the limitations of claim 28 as applied above. Further, Glenn discloses that said delay circuit performs said timing alignment by adjusting a first propagation delay circuit (fig. 4, ref. 407) coupled to a first transmission path (fig. 4, ref. 412) within said deskewing circuit by a first propagation delay value (fig. 4, ref. 410) and adjusting a second propagation delay circuit (fig. 4, ref. 408) coupled to a second transmission path (fig. 4, ref. 413) within said deskewing circuit by a second propagation value (fig. 4, ref. 411), wherein said first transmission path transports said source clock signal (fig. 4, "CLOCK") and said second transmission path transports said first data signal (fig. 4, "DATA").

Regarding claim 32, Glenn discloses the limitations of claim 28 as applied above. Further, Glenn discloses a phase locked loop circuit (fig. 4, refs. *the interconnections of 404-408*) which synchronizes said timing alignment by asserting a time dependent signal (fig. 4, refs. 416 and 417) aligned to said source clock signal to synchronize operation of said delay circuit (fig. 4, refs. 407 and 408; para. 0052) by the operative

interconnection of the elements of the deskewing circuit. That is, the phase locked loop is the particular sequence and connection of the elements of the deskewing circuit. It is a phase locked loop because the phase comparison by the PHASE ADJUSTMENT UNIT (fig. 4, ref. 405) is operatively connected to the PHASE SHIFTERS (fig. 4, refs. 407 and 408) which are operatively coupled to the DATA SAMPLER (fig. 4, ref. 404) providing a time dependent signal which is operatively coupled to the PHASE ADJUSTMENT UNIT *in a loop*.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen (U.S. 6801592 – previously cited).

Regarding claim 4, Glenn discloses the limitations of claim 3 as applied above. Glenn does not disclose that said first receiver and said second receiver each comprise a first receiver stage and a second receiver stage. However, Christensen teaches the use of input buffers to condition the input signals received. Christensen illustrates in figure 1 that a first receiver and said second receiver each comprise a first receiver stage (respectively 2 and 5) and a second receiver stage (respectively [3, 11, and 12] and [6-10]). Further, Christensen discloses that the first receiver stage (fig. 1, ref. 5) of the first receiver and the first receiver stage (fig. 1, ref. 2) of the second receiver each

comprise a signal conditioner or buffer (col. 5, lines 60-63; col. 6, lines 10-15). The data buffers taught by Christensen can be utilized to interface voltage levels and provide signal strength for the receiver's second stages. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize buffers as taught by Christensen as first receiver stages with Glenn's second receiver stages because they could interface voltage levels between the first and second receivers and provide signal strength for the received signals.

Regarding claim 5, Glenn in view of Christensen disclose the limitations of claim 4 as applied above. Further, Christensen discloses that the first receiver stage (fig. 1, ref. 5) of the first receiver and the first receiver stage (fig. 1, ref. 2) of the second receiver each comprise a signal conditioner or buffer (col. 5, lines 60-63; col. 6, lines 10-15). Further, it is implied that the output of a buffer has a fixed output as understood by one having ordinary skill in the art, and, as broadly as claimed, it is implied that the first receiver stages would both utilize a common voltage or have a common mode voltage.

10. Claims 12, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn in view of Flora et al (US 4755704; hereafter "Flora" – previously cited).

Regarding claim 12, Glenn discloses the limitations of claim 1 as applied above. Glenn discloses that the first and second receivers are first and second integrated circuit chips (para. 0002) but does not disclose that they are very large scale integration circuits. However, VLSI circuits are notoriously known in the art, and one skilled in the art is well aware that VLSI circuits provide the benefits of large circuits applied in a small

area having high speed and low power. Flora discloses the use of VLSI circuits in a clock de-skewing circuit (col. 2, lines 35-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize the notoriously known integrated circuit implementation of VLSI as disclosed by Flora for the integrated circuits of Glenn because they provide the benefits of large circuits applied in a small area having high speed and low power.

Regarding claim 16, Glenn discloses the limitations of claim 1 as applied above. Glenn discloses the transmitting and receiving circuits, but does not explicitly disclose that the circuits are mounted to a printed circuit board. The use of printed circuit boards are notoriously known in the art for mounting integrated circuits. Flora illustrates a notoriously known printed circuit board (fig. 1, ref. 2) with various integrated circuits mounted upon it (fig. 1, ref. 5; col. 3, lines 30-68). One skilled in the art would have been motivated to mount an integrated circuit to a printed circuit board as illustrated by Flora because a printed circuit board allows many integrated circuits to communicate and provide power. Further, as known by one having skill in the art, a printed circuit board can be utilized to provide utility for an integrated circuit by allowing it to be wired into a circuit (i.e. to use it). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to mount the integrated circuits of Glenn to a printed circuit board as taught by Flora because, among other reasons, it would allow the integrated circuits to be connected to additional circuits.

Regarding claim 17, Glenn discloses the limitations of claim 1 as applied above. Glenn discloses the first and second circuits, but does not explicitly disclose that the first

and second circuits are mounted to first and second printed circuit boards. The use of printed circuit boards are notoriously known in the art for mounting integrated circuits. Flora illustrates notoriously known printed circuit boards (fig. 1, ref. 2) with various integrated circuits mounted upon them (fig. 1, ref. 5; col. 3, lines 30-68). One skilled in the art would have been motivated to mount an integrated circuit to a printed circuit board as illustrated by Flora because a printed circuit board allows many integrated circuits to communicate and provide power. One skilled in the art would find it obvious to mount one integrated circuit to one board and another integrated circuit to another board as illustrated because one printed circuit board may not be large enough to mount a large number of integrated circuits. Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to mount the first integrated circuit of Glenn to a first printed circuit board as taught by Flora and the second integrated circuit to a second printed circuit board, because among other reasons, it would allow the integrated circuits to be connected to each other by a connection between the two printed circuit boards in the case that one circuit board may not accommodate enough integrated circuits.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn in view of Donnelly et al (U.S. 6539072; hereafter "Donnelly").

Regarding claim 15, Glenn discloses the limitations of claim 14 as applied above. Glenn discloses that the delay locked loop comprises a phase or delay shifter (fig. 4, refs. 407 and 408) to generate an output signal proportional to a control voltage (fig. 4. refs. 410 and 411) asserted by a loop filter (fig. 5, refs. 502a and 502b). Glenn does not

explicitly disclose that the delay locked loop comprises a voltage-controlled delay line. However, Donnelly teaches a delay locked loop circuit for delay adjustment (fig. 3). The delay locked loop comprises a voltage-controlled delay line (fig. 3, ref. 205) to accurately control the delay of an input signal (fig. 3, ref. 200) according to a control signal (fig. 3, ref. 260; col. 4, lines 25-35). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a voltage-controlled delay line as taught by Donnelly as the delay shifters of Glenn because they could be utilized to accurately control the delay of the received signals using a control voltage.

Allowable Subject Matter

12. Claims 18-27 are indicated to contain allowable subject matter.

13. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 18-27, the indication of allowable subject matter is made over the prior art of record because the prior art of record does not disclose or obviate the use of two delay lines utilized on the receiving side of a synchronous link to adjust the timing of the data and clock signals of the synchronous link individually to create a proper timing alignment between the data and clock signals.

14. Claims 9, 11, and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
October 26, 2005

jmp

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER